REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 29 to recite that the cavity has a plurality of gates formed on one side, of the opposed two sides, of the cavity of the molding die, and a plurality of air vents formed on the other side of the two sides; and to recite that in the block molding step the resin is injected into the cavity from the gates on the one side to the air vents on the other side. Claim 39 has been amended in light of amendments to claim 29, to recite the plurality of air vents.

In addition, Applicants are adding new claims 63-66 to the application. Claim 63, dependent on claim 60, recites that of the four sides of the cavity, two are longer than the other two, with the two sides respectively having the plurality of gates and the side opposite thereto being the two longer sides. Claim 64, dependent on claim 29, recites that the cavity has additional sides to the two sides, with the two sides being longer than the additional sides. Claim 65, dependent on claim 29, recites that after the step of mounting, at least fats and oils are on the main surface of the substrate, with the fats and oils being removed by the treating step by plasma; and claim 66, also dependent on claim 29, recites that in the block molding step the resin is injected from the gates on the one side so as to flow along the main surface of the substrate. In connection with amendments to the previously considered claims, as well as in connection with the newly added claims, note, for example, Fig. 6 and the description corresponding thereto in paragraphs [0064] and [0065] on pages 17 and 18 of Applicants' Substitute Specification submitted with the Preliminary Amendment filed

January 28, 2002. See also paragraph [0076] on page 23 of Applicants' Substitute Specification.

Applicants respectfully submit that all of the claims present in the above-identified application patentably distinguish over the teachings of the references applied by the Examiner in the Office Action mailed March 3, 2004, that is, the teachings of the U.S. patents to Tsuruta, No. 6,200,121, to Hashimoto, No. 5,729,437, to Miyajima, No. 6,344,162, and to Ishikawa, No. 5,939,792, under the provisions of 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of manufacturing a semiconductor device as in the present claims, including, inter alia, mounting a plurality of semiconductor chips on a plurality of product forming areas, arranged in a matrix, on a main surface of a substrate; after the mounting step, treating the main surface of the substrate by plasma; after the treating step by plasma, arranging the substrate in a molding die with the plurality of semiconductor chips being positioned in a cavity of the molding die and the plurality of product forming areas facing to the cavity; and after arranging the substrate in the molding die, block molding a resin enclosure by injecting resin into the cavity, with the cavity having two sides opposed to each other, a plurality of gates formed on one side, of the two sides, and a plurality of air vents formed on the other side of the two sides, and wherein in the block molding step the resin is injected into the cavity from the gates to the air vents. See claim 29.

As will be developed further infra, it is respectfully submitted that the present invention addresses the problem of voids being formed in the resin enclosure

particularly at a location behind the semiconductor chips in the direction of flow of the resin during the block molding (that is, flow from the gates on one side of the cavity to air vents on the opposed side of the cavity, as in claim 29, especially where the resin is injected so as to flow along the main surface of the substrate, as in claim 66); and particularly in view of this problem addressed by the present invention and the solution thereto, including, inter alia, the treating step by plasma with the molding die used, the references as applied by the Examiner would have neither taught nor would have suggested the present invention as a whole, including the problem addressed and source thereof, and the specific solution to this problem. In connection therewith, note particularly claims 31, 40, 49-51, 57, 58, 61, 62, 65 and 66.

In addition, it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, such method as in the present claims, having features as discussed previously, and additionally wherein the cavity has additional sides which also have air vents (see claims 55 and 59), more particularly, wherein the cavity has four sides in total, including the two sides opposed to each other and defined in claim 29, and an additional two sides opposed to each other, the four sides forming a quadrilateral, and wherein the additional two sides also have air vents (see claims 56, 60 and 63); or wherein the cavity has additional sides, the sides having the gates and air vents being longer than the other sides (see claims 63 and 64).

Furthermore, it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, such a method of manufacturing a semiconductor device as in the present claims, having features as discussed previously, and moreover wherein the resin enclosure includes a plurality of

fillers (see claims 34 and 43), in particular wherein a volume content of the plurality of fillers in the resin enclosure is more than 80 volume percent (see claims 35 and 44), and wherein the plurality of fillers are comprised of silica fillers (see claims 36 and 45). When using a resin sealing material containing a large amount of filler, the problem of voids is even greater; but such problem of voids is still avoided, even with use of a resin sealing material containing a large amount of filler, by the process according to the present invention.

Moreover, it is respectfully submitted that the teachings of the applied prior art would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining, dependent claims, having features as discussed previously, and further including (but not limited to) wherein in the treating step by plasma, impurities remaining on the main surface of the substrate are removed (see claims 31 and 40; note also claim 65), or the main surface of the substrate is roughened (see claims 32 and 41); and/or wherein in the mounting step, the substrate is heat treated (see claims 38 and 47); and/or wherein in the block molding step, a peripheral space of the cavity is provided between the plurality of product forming areas and the air vents, with a width of the peripheral space being larger than a width of spaces between the plurality of the product forming areas in plan view (see claim 39).

The present invention is directed to a technique particularly suitable for manufacture of semiconductor devices using block molding by transfer molding (e.g., injecting resin into a mold cavity). In the manufacture of semiconductor devices, a first technique for packaging semiconductor chips is to mount a plurality of semiconductor chips on a main surface of a substrate, block-molding the mounted semiconductor

chips on the substrate with one resin enclosure, by injection molding, and then separating the plurality of semiconductor chips from each other by cutting the resin enclosure and the substrate into respective devices (thus, for example, a single semiconductor chip or stacked semiconductor chips within each respective package is formed).

A second technique, involving a different technology having different problems and different solutions, includes a potting method. For example, in potting, a problem arises in that air bubbles form in the potted enclosure; however, in such potting, the air bubbles can be removed by placing semiconductor devices, that are in a state in which the resin has not been cured, in a low-pressure atmosphere after potting. In transfer molding, resin injection and curing are performed inside a cavity, and thus the method for reducing voids by vacuum defoaming, which can be used in a potting method, cannot be adopted.

In connection with using block molding by transfer or injection molding, and as found and investigated by the Applicants, and as shown in Figs. 23A to 26B and described in the corresponding description in paragraphs [0004] to [0009] on pages 2-4 of Applicants' Substitute Specification, there arises a specific problem when block transfer molding is used in forming a plurality of semiconductor devices in one resin enclosure. Such problem occurs with flow of resin from one side to an opposed side of the cavity in which the block transfer molding occurs. It is emphasized that this problem occurs in such block transfer molding, and that there is no disclosure that such problem occurs in potting molding. In performing the block molding by injecting resin into a cavity, the flow of the resin 67A (note the aforementioned Figs. 23A to 26B)

along the main surface of the semiconductor chip 61 is resisted by the semiconductor chip. Therefore, the resin formed along the main surface of the chip runs slower than the resin 67A flowing along the side surfaces of the semiconductor chip (see Figs. 24A and 24B). For these reasons, voids 67B tend to be generated at positions where the resin 67A flowing along the main surface of the semiconductor chip 61 meets the resin 67A flowing along the side surfaces of the semiconductor chip 61 (see Figs. 25A and 25B). Particularly troublesome are voids 67C remaining at positions hiding behind the semiconductor chips 61 with respect to the injecting direction S of the resin 67A (see Figs. 26A and 26B). These voids, e.g., voids 67C, are a factor that reduces yield of semiconductor devices.

This problem of voids is even greater when a great amount of filler (for example, 80% or more) is added to the molding resin, e.g., for purposes of reducing warpage due to the shrinkage of the molding resin, to facilitate the dicing process, or for providing a more compatible thermal expansion coefficient of the resin to that of the semiconductor chip. That is, in including a large amount of filler, a thixotropic property cannot be used to remove/avoid voids.

Against this background, the present inventors turned their attention to the wettability of the resin 67A to the main surface of the substrate, and based thereon, have achieved the present invention which overcomes problems of voids, especially in connection with block molding by injection of resin into die cavities, where the die cavities have gates at one side of the cavity and air vents on an opposed side, and with, e.g., flow of the resin being parallel to the main surface of the substrate. Note

paragraph [0014] on page 6 of Applicants' Substitute Specification. That is, Applicants have found that voids in the resin, arising during the block transfer molding by injection of resin, becomes more easily removed from a main surface of a substrate in the step of transfer molding, by performing a plasma treatment of the main surface before the block molding step, the plasma treatment enhancing wettability of the resin to the main surface of the substrate, e.g., by cleaning the substrate and roughening the substrate, after mounting the semiconductor chips on the substrate.

That is, as described, for example, from paragraph [0067] through paragraph [0070] on pages 18-20 of Applicants' Substitute Specification, during the mounting procedure the substrate is heated and impurities such as fats, oils and organic solvents are outgassed so as to contaminate the main surface of the substrate. Performing the plasma treatment removes impurities, such as fats and oils; and, moreover, can roughen the surface of the substrate, all increasing wettability thereof. Since these impurities have been removed, the resin from along the side surfaces of the semiconductor chip 10 is allowed to easily enter positions, e.g., behind the semiconductor chips with respect to the injecting direction S of the resin 24A (see, e.g., Figs. 14A and 14B of Applicants' disclosure). As a result, the voids 24B generated at the positions where the resin 24A flowing along the main surface of the semiconductor chip 10 meets the resin 24A flowing along the side surfaces of the semiconductor chip 10 are dislodged, and the voids thus dislodged are able to easily move in response to the flow of the resin in the resin injecting process. Therefor, the voids do not remain at positions behind the chips; and, thus, problems due to such voids can be avoided.

Tsuruta discloses a process for molding semiconductor chips, and a molding die used therein. The process includes steps of preparing a circuit panel having plural conductive patterns formed on an insulating layer and plural semiconductor chips mounted on the circuit panel and electrically connected to the plural conductive patterns, respectively; accommodating the semiconductor chips mounted on the circuit panel in a cavity of a molding die having a gate extending along one of peripheral lines defining the cavity; supplying melted synthetic resin through the gate into the cavity so as to fill the vacant space of the cavity therewith; solidifying the melted synthetic resin; and cutting the large piece of synthetic resin so that the semiconductor chips are sealed in small pieces of synthetic resin, respectively. See column 3, lines 29-45. Looking to Figs. 4 and 5, and the description in connection therewith in columns 5 and 6, this patent discloses dummy cavity 21g in parallel to the gate 21b; the dummy cavity 21g is effective against wire weep and voids, in that resin injected from the gate 21b falls into dummy cavity 21g so that synthetic resin in cavity 23 is not subjected to turbulence.

It is respectfully submitted that this patent does not disclose, nor would have suggested, the problem addressed by Applicants, of voids (in sealing resin formed by block molding a plurality of chips within a single resin block which is later cut) due to flow of resin along the chips, and particularly voids formed behind chips in the direction of resin flow; and would have neither disclosed nor would have suggested the solution to this problem of voids, as discovered by Applicants, of conducting the plasma treatment after mounting and prior to block molding; or the particular molding die used, which, e.g., gives rise to the problem.

In particular, it is emphasized that Tsuruta requires the dummy cavity, and it is respectfully submitted that this reference does not disclose, nor would have suggested, the air vents as in claim 29, much less the air vents as in claims 55, 56, 59 and 60. In this regard, note that Tsuruta, in plan view, does not even show the end sides of the molding die. Clearly, Tsuruta is not concerned with any air vent structure, and does not disclose, nor would have suggested, use of the molding die as in the present claims, having the recited air vents as in claim 29, and especially having the structure of air vents in sides of the cavity as in claims 55, 56, 59 and 60.

Moreover, clearly Tsuruta does not disclose, nor would have suggested, the plasma treatment after the mounting step, and prior to the block molding by injecting resin, and advantages thereof, especially in solving the problem addressed by the present invention. In this regard, it is again emphasized that Tsuruta does not disclose, nor would have suggested, the problem addressed by the present invention, of voids due to differential flow of resin at the semiconductor chips, nor would have disclosed or suggested the solution of this problem. Again emphasizing that the present invention as a whole must be considered, including the problem addressed and solved, and source of this problem, clearly the teachings of Tsuruta are deficient with respect to the presently claimed subject matter.

It is noted that while Tsuruta discloses a problem of voids when injecting molten resin into a cavity through plural gates, e.g., at column 3, lines 17-23 of this patent, Tsuruta discloses avoiding such voids through use of the united long injection gate (narrow gap 21d) and dummy cavity 21g, to smooth resin flow and solve the problem of the void. See column 6, line 49, to column 7, line 6 of Tsuruta. Accordingly, by way of

the disclosure of Tsuruta, the problem of voids described therein has been solved; note also that Tsuruta does not disclose a plasma treatment, much less that such plasma treatment is effective to solve a problem of voids.

In contrast, the void problem described in the above-identified application is effectively solved by applying the plasma treatment with the resin flow according to the present invention, from gates in the side of the cavity to the air vents at least at an opposed side of the cavity. The void problem described in the present application is effectively solved according to the present invention, without the need of the united long injection gate and dummy cavity as in Tsuruta. In this regard, note that the united long injection gate and dummy cavity as in Tsuruta have disadvantages in occupying large areas of the substrate and decreasing an available area in the cavity for structure to be molded. It is respectfully submitted that the present invention, as compared with Tsuruta, has the advantage of enlarging an available area of the substrate for product formation.

In addition, the present inventors have found that the united long injection gate and dummy cavity as disclosed in Tsuruta are not sufficient countermeasures against the void problem, described in the present application because even when using the long gate and dummy cavity the resin flow is disturbed by the mounted chips, making it difficult to completely eliminate voids in the resin (that is, voids might remain at positions hiding behind the semiconductor chips).

In contrast, the present invention is effective in removing voids from a main surface of a substrate and allowing the voids to easily move by the flow of the resin in the resin injecting process, so that the voids do not remain at positions hiding behind

the semiconductor chips. The voids become sufficiently small, according to the present invention, to the extent that the popcorn phenomenon (damage caused by explosion of moisture trapped in the voids) can be avoided. Note paragraph [0075] on pages 22 and 23 of Applicants' Substitute Specification.

As can be seen in the foregoing, while Tsuruta addresses a problem of voids, it would have neither disclosed nor would have suggested the problem addressed by the present invention, and clearly would have neither taught nor would have suggested the solution thereto as achieved by the present invention. To emphasize, noting that Tsuruta generally discloses avoiding voids, it is respectfully submitted that the reference would not have taught the specific problem addressed by the present invention, of the specific type of voids, and the solution thereto as achieved according to the present invention.

It is respectfully submitted that the additional teachings of Hashimoto and of Miyajima would not have rectified the deficiencies of Tsuruta, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art. In particular, and as will be discussed infra, it is respectfully submitted that the combined teachings of Hashimoto, Miyajima and Tsuruta would have neither taught nor would have suggested the problem addressed according to the present invention and solution thereto, achieved according to the present invention.

Hashimoto discloses a method of manufacturing electronic parts, including a substrate manufacturing step for forming throughholes in a substrate material along lattice-like imaginary lines, the throughholes being caused to have external electrodes formed by cutting the throughholes along centers thereof; a mounting step for mounting

element parts in regions of the substrate material surrounded by the imaginary lines; a connection step for establishing electrical connecting among the element parts and the corresponding throughholes; a molding step for introducing molding resin into the entire surface of the substrate material to mold the element parts; and a cutting step for cutting the substrate material, the molding resin and the throughholes along the imaginary lines after the molding resin has been hardened. See column 3, lines 41-55. Note also column 4, lines 33-43, disclosing use of a closing member for closing an opening portion of each of the throughholes prior to performing the molding step, and an opening step for removing the closing member after the molding resin has been hardened. This patent further discloses injection of conductive paste, e.g., solder paste, into the throughholes, to fill the throughholes with solder. See column 9, lines 24-45. Column 15, lines 3-20, of this patent discloses that if potting molding is employed, generation of portions that are not filled with molding resin 5 can be prevented completely by performing vacuum defoaming in the process for applying the molding resin; and that when using potting molding, if the surfaces of the substrate 6 and the semiconductor device 1 are activated with oxygen or argon plasma immediately before the process for applying the molding resin 5, further excellent contact of the molding resin 5 can be established.

It is emphasized that Tsuruta discloses the use of a specific die structure for avoiding, inter alia, voids in the formed resin. In contrast, Hashimoto discloses a potting technique including activation of surfaces of the substrate with oxygen or argon plasma immediately before the process for applying the molding resin, to establish contact of the molding resin. See column 15, lines 3-20. It is respectfully submitted

that, apart from Applicants' disclosure, there would have been no motivation and/or suggestion from the teachings of Tsuruta and/or Hashimoto, or of the other applied references, for combining the teachings of these references as applied by the Examiner. Emphasizing that Hashimoto discloses an activation with oxygen or argon plasma, it is respectfully submitted that the teachings of this reference, either alone or in combination with the teachings of the other references as applied by the Examiner, would have neither taught nor would have suggested the cleaning according to the present invention, much less use of such cleaning to help remove the voids, and advantages thereof as achieved according to the present invention. Especially noting that Tsuruta provides a specific technique for avoiding problems of voids, it is respectfully submitted that the Examiner has pointed to no proper motivation for combining the teachings of the applied references.

The contention by the Examiner in the first four lines on page 3 of the Office Action mailed March 3, 2004, that it would have been obvious to clean the substrate taught by Tsuruta prior to encapsulation to improve the contact of the molding resin and thus reliability of the electronic part as taught by Hashimoto, is noted. It is emphasized, however, that Hashimoto does not disclose plasma treatment for cleaning; only Applicants' original disclosure teaches cleaning by the plasma treatment. In contrast, note that Hashimoto discloses "activation" with oxygen or argon plasma. Noting that the Examiner is relying on cleaning for motivation, it is respectfully submitted that the Examiner is using Applicants' original disclosure against Applicants, in coming to a conclusion of obviousness, clearly improper under the guidelines of 35 USC §103.

Moreover, note that the present claims recite that the main surface of the substrate is treated by plasma after the mounting step. It is to be noted that according to the present invention, various impurities may be outgassed from the substrate by, e.g., heating during the mounting step. Even taking the teachings of the references as applied by the Examiner, it is respectfully submitted that the combined teachings of the references would have neither disclosed nor would have suggested the specific sequence of processing steps as in the present claims.

Even taking the teachings of Miyajima in combination with the teachings of Tsuruta and Hashimoto, it is respectfully submitted that the combined teachings of these references would have neither disclosed nor would have suggested the presently claimed subject matter, including, inter alia, the plurality of gates and plurality of air vents on opposite sides of the cavity, and/or flow of resin as in the presently claimed method, with problems arising due to voids in connection therewith, and avoidance of such problems as achieved according to the present invention.

Miyajima discloses a method of manufacturing semiconductor devices in a molding machine including an upper die and a lower die, in one of which dies a plurality of cavities corresponding to resin-molded parts of the semiconductor devices are formed. The method includes steps of covering inner faces of the cavities and a parting face of one of the dies, which contacts a substrate of the semiconductor devices, with a release film, which is easily peelable from the dies and resin for molding; clamping the substrate with the dies; fitting the resin in the cavity; and forming the semiconductor devices by cutting the molded substrate. See column 1, line 56, to column 2, line 2. The main characteristic of the resin molding machine according to Miyajima is use of

the release film; by use thereof, the resin in each cavity space is properly pressurized by air pressure of the air left in the cavity space and the elasticity of the release film. Note column 15, lines 22-27. As applied by the Examiner, this reference discloses a resin molding machine having an overflow cavity 102 (note Figs. 19A and 19B) communicated to an air mechanism via air paths 104. Reference character 106 in these figures stands for an overflow gate, and reference character 108 stands for air vents. This patent discloses that the overflow cavity 102 is formed like a ring-shaped groove, with the overflow gate 106 formed on the inner side thereof and the air vents 108 being radially outwardly extended from the overflow cavity 102 with regular separation. Note column 14, lines 17-30.

As can be appreciated from the foregoing, the overflow cavity in Miyajima is formed like a ring-shaped groove, with the air vents being radially outwardly extended therefrom. Taking the teachings of Miyajima as a whole, together with the teachings of Hashimoto and Tsuruta, it is respectfully submitted that the combined teachings of these references would have neither disclosed nor would have suggested the molding die structure as in the present claims, having the two sides opposed to each other with a plurality of gates formed on one side, of the two sides, and a plurality of air vents formed on the other side of the two sides, with injection of the resin, as in claim 29, and, in particular with flow of the resin as in claim 66, in combination with use of the treating step by plasma which avoids the specific void problem, as discussed previously.

The contention by the Examiner in the second full paragraph on page 3 of the Office Action mailed March 3, 2004, that Miyajima teaches the use of air vents with

regions 102 (which are similar in nature to dummy gate regions 21g of Tsuruta), is noted. It must be emphasized, however, that Miyajima discloses air vents extending radially outwardly from the overflow cavity which is formed like a ring-shaped groove. Taking the disclosure of Miyajima as a whole, as required under the requirements of 35 USC §103, even in combination with the teachings of Hashimoto and Tsuruta, it is respectfully submitted that the combined teachings of these references do not disclose, nor would have suggested, positioning of the gates and of the air vents as in the present claims, with injection and flow of resin as in the present claims, and particularly problems arising in connection therewith; and wherein use of the plasma treatment with the use of the defined molding die as in the present claims avoids the void problems, providing advantages achieved by the present invention.

The additional contention by the Examiner in the last paragraph on page 3 of the Office Action mailed March 3, 2004, that Hashimoto teaches in column 13 that heating during the mounting step allows conductive paste to flow, and upon cooling to attach to surfaces, such that the use of a heating step during the mounting would be an inherent part of the bumping method taught by Tsuruta, is noted. However, it must be emphasized that, as described in Applicants' original disclosure, the heating step causes impurity problems which, during the block molding, can cause voids hiding behind the chips to form, which voids are avoided according to the present invention. Taking the present invention as a whole, including the problem discovered, source of such problem and solution thereto, it is respectfully submitted that the description of a heating step in the potting method of Hashimoto would have neither disclosed nor would have suggested, either alone or in combination with the teachings of the other

applied references, the present invention, including the problem addressed and source thereof, and discovery of the solution to this problem.

It is respectfully submitted that the additional teachings of Ishikawa would not have rectified the deficiencies of the teachings of Tsuruta, Hashimoto and Miyajima, even if the teachings of the references were properly combinable, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Ishikawa discloses a resin-mold type semiconductor device packaged with an epoxy-based resin, and a manufacturing method therefor. The method includes steps of supporting and fixing a semiconductor chip on a die pad; electrically connecting distal end portions of a plurality of inner leads which face the semiconductor chip to a plurality of terminal electrodes of the semiconductor chip by bonding wires, respectively; molding the die pad, the semiconductor chip, the plurality of inner leads and the bonding wires in a resin mold which is made of a sealing resin; and forming a highly water-absorbent insulating film made of a highly water-absorbent polymer on a surface of the resin mold. See column 3, lines 50-63. In column 6, lines 60-67, the sealing resin is disclosed as an epoxy resin containing a silica filler in an amount of 70-80% by weight based on the overall weight of the resin-mold package.

Even assuming, arguendo, that the teachings of Ishikawa were properly combinable with the teachings of the other references as applied by the Examiner, it is respectfully submitted that such combined teachings would have neither disclosed nor would have suggested the void problem which is especially severe when using a sealing resin containing relatively large amounts of filler; would have neither disclosed

nor would have suggested the source of this problem of voids, particularly voids hiding behind the semiconductor chip in the direction of resin flow; and would have neither taught nor would have suggested the solution to this problem of applying the plasma treatment after the mounting step, using the molding die as in the present claims having a cavity with two sides opposed to each other respectively having a plurality of gates and a plurality of air vents, with the resin being injected into the cavity from the gates on the one side to the air vents on the other side. Moreover, it is respectfully submitted that the combined teachings of these references would have neither disclosed nor would have suggested the other aspects of the present invention as in the present claims as discussed previously, and advantages achieved thereof.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.40695X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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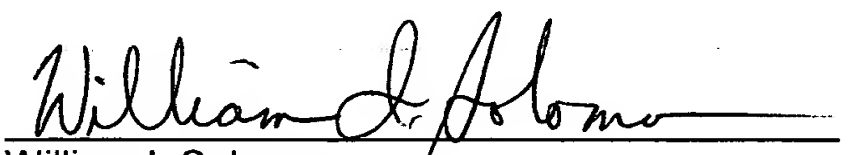

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